EE/CprE/SE 491 WEEKLY REPORT 5

Date: ***Feb 27th, 2023 – Mar 5th, 2023***

Group number: ***sddec23-08***

Project title: ***ReRAM Compute ASIC Fabrication***

Client &/Advisor: ***Henry Duwe & Cheng Wang***

Team Members/Role:

- ***Josh Thater - Mixed Signal Designer***
- ***Matt Ottersen - VLSI Designer***
- ***Aiden Petersen - Digital Designer***
- ***Regassa Dukele - VLSI Designer***

Weekly Summary

For the fifth week, we got more acquainted with the open-source tools and how they fit in with the Efabless process. Last week, we were able to obtain a branch of a Git repository that fixed the analog Caravel framework, so this week, we tested things within it and troubleshot some reaming issues. We also began documenting the process as well as creating a flowchart to help outline how the process flow works so that future students will have an easier time with similar projects. We also got more comfortable with Xschem and testing the schematic within NGSpice.

Past week accomplishments

- Joshua Thater
    - Shared VM environment with team that contained tools and dependencies
    - Continued to write out documentation on the analog process
    - Simulated and ran precheck on analog user project
- Aiden Petersen
    - Create flowchart for toolflow for organization purposes
- Matt Ottersen
    - Ran simulations using skywaters logic gates in ngspice
    - Started to research creating a layout in magic
- Regassa Dukele

- Created a personal VM environment that works with my machine/laptop

Pending issues

- Creating a sample project to simulate and pass precheck with
- How to upload spice netlist into Magic
- How we connect our design to the overall Caravan harness

Individual contributions

Team Member	Individual Contributions	Weekly Hours	Total Hours
Joshua Thater	Created VM environment and continued documentation	4	31
Aiden Petersen	Create flowchart for toolflow	2	27
Matt Ottersen	Simulated skywater Logic gates	6	27
Regassa Dukele	Created a personal VM environment	7	28.5

Plans for the upcoming week

- Joshua Thater
  - Try to finish up documentation on steps for how to configure all tools and dependencies on a brand new Ubtuntu VM
  - Make a basic DAC and try to get it through the entire process flow
- Aiden Petersen
  - Better understand the verification process
  - Start understand wishbone bus interaction with caravel MCU
- Matt Ottersen
  - Create a layout from a schematic
  - Make and simulate a basic ADC
- Regassa Dukele
  - Run the test on my created virtual machine
  - Start working on the ADC circuit.